IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Thomas P. Glenn et al.		
Assignee:	Amkor Technology, Inc.		
Title:	WAFER HAVING BACK-SIDE ALIGNMENT MARKS		
Serial No.:	09/803,084	Filed:	March 8, 2001
Examiner:	Williams, Alexander O.	Group Art Unit:	2826
Docket No.:	G0049		

Monterey, CA
April 4, 2003

CLEAN COPY OF REPLACEMENT CLAIMS

Replace the pending set of claims in the above application with the following set of claims:

1. A wafer comprising:

a first surface;

a second surface;

a first scribe line coupled to said first surface, said first scribe line extending in a first direction;

a second scribe line coupled to said first surface, said second scribe line extending in a second direction perpendicular to said first direction; and

a first alignment mark formed at an intersection of said first scribe line and said second scribe line, said first alignment mark extending from said first surface to said second surface.

2. The wafer of Claim 1 further comprising a scribe grid comprising said first scribe line and said second scribe line.

3. The wafer of Claim 2 further comprising electronic components delineated by said scribe grid.

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4. The wafer of Claim 3 wherein said electronic components are selected from the group consisting of integrated circuits, micromachine chips and image sensor chips.

5. The wafer of Claim 3 wherein said electronic components comprise bond pads coupled to said first surface.

6. The wafer of Claim 3 wherein said electronic components comprise active areas coupled to said first surface.

7. The wafer of Claim 1 further comprising a flat extending in said second direction.

8. The wafer of Claim 1 wherein said first scribe line delineates a first electronic component from a second electronic component.

9. The wafer of Claim 8 wherein said second scribe line delineates said second electronic component from a third electronic component.

10. The wafer of Claim 1 wherein said first alignment mark is an aperture.

11. The wafer of Claim 1 further comprising a first plurality of alignment marks comprising said first alignment mark, said first plurality of alignment marks extending from said first surface to said second surface.

12. The wafer of Claim 11 wherein said first plurality of alignment marks are aligned with said first scribe line.

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13. The wafer of Claim 12 further comprising a second plurality of alignment marks aligned with a third scribe line coupled to said first surface and extending in said second direction.

14. The wafer of Claim 11 wherein said first plurality of alignment marks define a first line, said first line being aligned with said first scribe line.

15. The wafer of Claim 14 further comprising a second plurality of alignment marks defining a second line, said second line being aligned with a third scribe line coupled to said first surface and extending in said second direction.

23. (AMENDED) A wafer comprising:

a first surface;

a second surface;

a scribe grid coupled to said first surface; and

a plurality of alignment marks extending from said first surface to said second surface, said plurality of alignment marks having a positional relationship to said scribe grid.

24. The wafer of Claim 23 wherein said scribe grid comprises a horizontal scribe line, a first set of said plurality of alignment marks being aligned with said horizontal scribe line.

25. The wafer of Claim 24 wherein said scribe grid comprises a vertical scribe line, a second set of said plurality of alignment marks being aligned with said vertical scribe line.

30. (NEW) The wafer of Claim 2 wherein said scribe grid comprises an etched silicon oxide layer.

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31. (NEW) The wafer of Claim 23 wherein said scribe grid comprises an etched silicon oxide layer.

32. (NEW) The wafer of Claim 23 further comprising electronic components delineated by said scribe grid.

33. (NEW) The wafer of Claim 32 wherein said electronic components are selected from the group consisting of integrated circuits, micromachine chips and image sensor chips.

34. (NEW) The wafer of Claim 32 wherein said electronic components comprise bond pads coupled to said first surface.

35. (NEW) The wafer of Claim 32 wherein said electronic components comprise active areas coupled to said first surface.

36. (NEW) The wafer of Claim 25 wherein said vertical scribe line extends in a first direction and wherein said horizontal scribe line extends in a second direction, said wafer further comprising a flat extending in said second direction.

37. (NEW) A wafer comprising:

a front-side surface;

a back-side surface;

a first scribe line coupled to said front-side surface; and

a first back-side alignment mark extending from said front-side surface to said back-side surface, said first back-side alignment mark being formed along said first scribe line.

38. (NEW) The wafer of Claim 37 further comprising a plurality of back-side alignment marks extending from said front-side surface to said back-side surface, said plurality

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of back-side alignment marks comprising said first back-side alignment mark.

39. (NEW) The wafer of Claim 38 wherein said plurality of back-side alignment marks have a positional relationship to said first scribe line.

40. (NEW) A wafer comprising:

a first surface;

a second surface;

a scribe line coupled to said first surface; and

a means for determining a position of said scribe line from said second surface, said means for determining extending through said wafer from said first surface to said second surface.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on April 4, 2003.

Attorney for Applicant(s) April 4, 2003
Date of Signature

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